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Docket No.: GR 98 P 1507

Date: October 10, 2000

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Enclosed herewith are the necessary papers for filing the following application for Letters Patent:

Applicant : ANDREAS RUSCH ET AL.

Title : SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR FABRICATING IT

2 sheets of formal drawings in triplicate.
A check in the amount of \$ 710.00 covering the filing fee.
PCT Publication (cover sheet only).

This application is being filed without a signed oath or declaration under the provisions of 37 CFR 1.53(d). Applicants await notification of the date by which the oath or declaration and the surcharge are due, pursuant to this rule.

The Patent and Trademark Office is hereby given authority to charge Deposit Account No. 12-1099 of Lerner and Greenberg, P.A. for any fees due or deficiencies of payments made for any purpose during the pendency of the above-identified application.

Respectfully submitted,

For Applicants

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LAG:kc

PCT
WELTORGANISATION FÜR GEISTIGES EIGENTUM
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Veröffentlicht

Mit internationalem Recherchenbericht.
Vor Ablauf der für Änderungen der Ansprüche zugelassenen
Frist; Veröffentlichung wird wiederholt falls Änderungen
eintreffen.

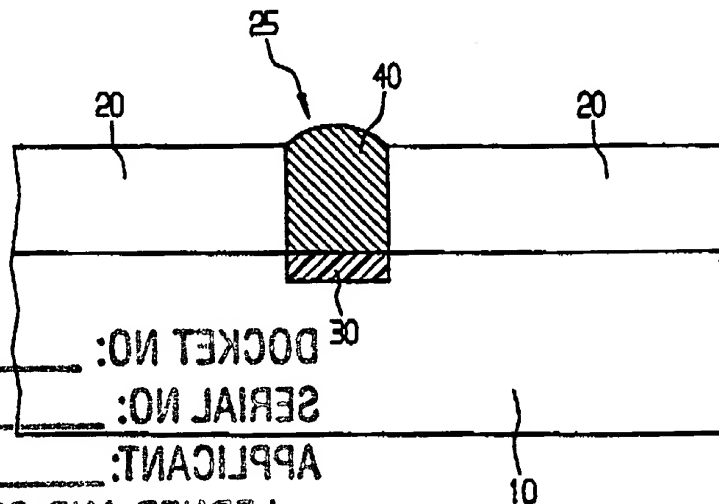
(54) Title: SEMICONDUCTOR MEMORY AND METHOD FOR PRODUCING SAME

(54) Bezeichnung: HALBLEITER-SPEICHERVORRICHTUNG UND VERFAHREN ZU DEREN HERSTELLUNG

(57) Abstract

The invention relates to a semiconductor memory with a matrix of semiconductor memory elements arranged in a substrate (10), which each comprise: a substrate area (10) of a first conductivity type; an insulating layer area (20) provided for on the substrate area (10); a via hole area (25) provided for in the insulating layer area (20); a bit fixing area (30) provided for in the substrate area (10) below the via hole area (25); and a contact pin area (40) which is provided for in the via hole area (25) and is in electric contact with the bit fixing area (30).

The bit fixing area (30) is configured in such a way that it fixes the contact resistance between the substrate area (10) and the contact pin area (40) in accordance with the bit to be fixed in each semiconductor memory element.



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